Sunplus SPT6601A Data Sheet

Preliminary

2001/04/30

Version 0.1

Table of Contents

PAGE

CALLER ID CONTROLLER/LCD DRIVER

1. GENERAL DESCRIPTION

The SPT6601A, a newly invented micro-controller for caller ID and vocal dialer products, carries SUNPLUS newest 16-bit *μ'nSP*™ CPU technology. The *μ'nSP*™ high processing speed assures that the SPT6601A is able to facilitate the sophisticated digital signal processing. In addition to the advanced *μ'nSP*™ technology, other primary functions include RAM, ROM, IO, interrupt controller, three timer/counters, LCD controller/driver, 8-bit Analog-to-Digital Converter (ADC), Dual-Tone-Multi-Frequency (DTMF) generator, and melody Digital-to-Analog Converter (DAC) output. For power savings, a software controllable standby mode and adjustable CPU clock can be used to achieve the best power management.

The SPT6601A is able to drive LCD directly, and to perform complex function and arithmetic. An external 32768Hz crystal oscillator produces a steady time base for clock function. With the built-in DTMF generator, the telephone dialer function can be implemented. Plus, the flexible LCD controller and regulator make the LCD driver achieving the best display quality.

The SPT6601A can be widely used in telecom products such as multifunction telephone dialer with/without Caller Identification and general-purpose controller. The SPT6601A provides, not only the latest telecom technology, but also the full service and support of SUNPLUS.

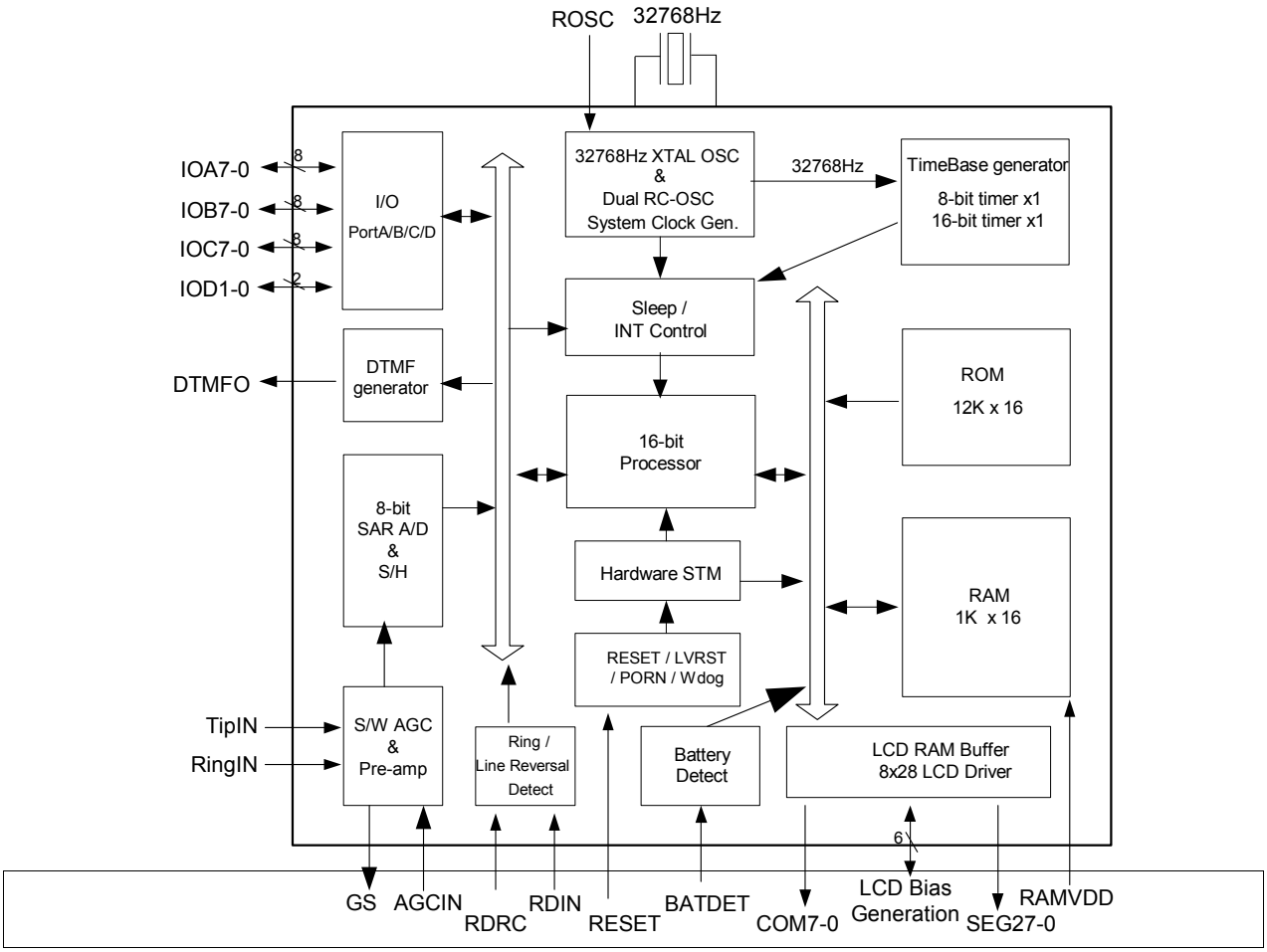
2. FEATURES

- SUNPLUS 16-bit *μ'nSP*™ CPU
  - SRAM 1K x 16 bits
  - ROM 12K x 16 bits
- Clock
  - An external 32768Hz crystal for dialing and demodulation
  - An external resistor to drive RC-oscillator for CPU clock
  - Programmable RC-oscillator frequency : 1.0MHz or 10.0MHz
  - /1,/2,/4,/8 of selected RC-oscillator for CPU clock
- Operating voltage
  - CPU operating voltage : 2.0V - 3.6V
  - DTMF receiver / FSK decoder : 2.2V - 3.6V
- Operation Modes
  - Operating mode, Standby mode, and Halt mode
- Timer/Counter
  - One 16-bit timer/counter
  - One 8-bit timer
- Power management for system reliability
  - Low-Voltage-Reset function
  - Power-On-Reset function
  - 8-level battery voltage detect
  - Watchdog reset (derived from 32768Hz crystal)
  - Independent power supply for SRAM to store call history
- Analog Front End
  - Op amp for the twisted pair telephone line
  - 4-level programmable AGC (1/2, x2, x8, x32)
  - 8-bit A/D, with sample-rate up to 8KHz
- Dialer
  - Built-in DTMF generator
- 10 Interrupt / Wakeup Sources (INT / WP)
  - IOC[1:0] edge-triggered
  - Ring signal Detect
  - IOA[7:0] edge-triggered
  - Timer A / Timer B overflow
  - T32KHz, T2KHz, T128Hz, T8Hz (derived from 32768Hz)
- LCD Driver
  - 8 COM x 28 SEG, 224 dots.
  - 1/4 bias, 1/8 duty
  - Built-in LCD voltage regulator
- Up to 26 I/O pins
  - IOA[7:0]:programmable pull-high, wakeup / interrupt
  - IOA[7:6]:programmable pull-high / pull-low, wakeup / interrupt
  - IOB[7:0]:COMS input / output, IOB[7:6] NMOS open drain
  - IOC[7:0]:COMS input / output, IOC[7:6] NMOS open drain
  - IOD[1:0]:CMOS input / output, IOD[1] tone output
- DTMF and FSK demodulation
  - Object code of DTMF and FSK decoders provided
  - Compatible with Bell 202, and ITU V.23 FSK specifications
  - FSK/DTMF decoder auto-select function
- Miscellaneous
  - Multiplication with cumulative addition for user's digital filters
  - Ring / Line Reversal Detector
  - DAC for melody and speech playback

3. APPLICATION FIELD

- Telephones, fax machines, answering machines, and modems that support caller-ID services
- Adjunct boxes for caller-ID information services

4. BLOCK DIAGRAM



5. SIGNAL DESCRIPTIONS

P: Port

Mnemonic	PIN No.	Type	Description
SEG[27:1] SEG0	27 - 1 86	O	LCD segment outputs
COM[7:0]	85 - 78	O	LCD common outputs
VLCD	74	O	LCD power supply. Connect a 0.1μF capacitor between this pin and VSS.
VDD[3:1]	73 - 71	O	LCD bias voltage, To regulate the LCD supply voltage, individually connect a 0.1μF capacitor between each pin and VSS.
CUP[2:1]	76 - 75	O	LCD charge pump capacitor interconnection pins. Connect a 0.1μF capacitor between CUP1 pin and CUP2 pin.
IOA[7:0]	53 - 60	I/O	8-bit I/O port, Each pin could be set as an input or output individually Input mode: Each one of IOA[5:0] is a CMOS input with programmable internal pull-high resistor, Moreover, each one of IOA[7:6] is a COMS inputs capable of both programmable pull-high and pull-low resistors. Output mode: CMOS output All pins are capable of wake-up and interrupt functions.
IOB[7:0]	44 - 51	I/O	8-bit I/O port, Each pin can be set as an input or output individually Input mode: Each one of IOB[7:0] is a CMOS input pin without internal pull resistor Output mode: IOB[5:0] are conventional CMOS outputs, whereas IOB[7:6] are NMOS open drain outputs.
IOC[3:0] IOC[7:4]	40 - 43 30 - 33	I/O	8-bit I/O port. Each pin can be set as an input or output individually Input mode: conventional CMOS inputs without internal pull resistors, Moreover, IOC[1:0] provide wake-up and interrupt functions enabled by software. Output mode: IOC[5:0] are CMOS outputs and IOC[7:6] are NMOS open drain outputs
IOD[1:0]	28 - 29	I/O	2-bit I/O port. Each pin can be set as an input or output individually. Input: pure input without pull-low / pull-high Output: CMOS output, IOD[1] can be programmed as tone output. Its frequency depends on the time-out signal of up-count Timer A or Timer B.
ROSC	35	I	RC-oscillator resistor interconnection pin, Connect a resistor between this pin and VDD.
TEST	36	I	Test input pin. It is internally pulled low.
X32O	37	I	32768Hz crystal oscillator output
X32I	38	O	32768Hz crystal oscillator input
RESET	39	I	System reset input. It is low-active and internal pulled high. All of the internal registers are reset to the default state when this pin is set to Low level. Connect a 0.1μF capacitor between this pin and VSS to achieve power-on reset.
RDIN	68	I	Ring detector input It is a Schmitt trigger input. Attenuate the incoming ring signal by placing 2-resistor ladder at this pin.
RDRC	67	I	Ring detector RC-delay input It is an open-drain output of Schmitt trigger at RDIN pin, and meanwhile another Schmitt trigger input. Connect an RC-network to this pin to set the delay time for ring detection.

Mnemonic	PIN No.	Type	Description
TIPIN	63	I	Positive input of pre-amplifier Connect this pin to the TIP side of the twisted-pair telephone line through a 150KΩ resistor and a DC-decoupling capacitor. Besides, connect a 1000-pF capacitor between this pin and AVSS to improve noise immunity.
RINGIN	64	I	Negative input of pre-amplifier Connect this pin to the RING side of the twisted-pair telephone line through a 150KΩ resistor and DC-decoupling capacitor. Besides, connect a 1000-pF capacitor between this pin and GS pin to improve noise immunity.
GS	65	O	Output of pre-amplifier Connect a 0.1μF capacitor between this pin and AGCIN pin to block DC bias between the pre-amplifier and AGC. Also, connect a 1000-pF capacitor between this pin and RINGIN.
AGCIN	66	I	AGC input
DTMFO	62	O	DTMF tone output
BATDET	69	I	Battery voltage detect input
AVDD	70	I	Analog circuit power input
AVSS	61	I	Analog circuit ground input
VDD	34	I	Digital circuit power input
RAMVDD	77	I	SRAM power input, To avoid SRAM data lost while entering low-power reset state, connect a Schottky diode between this pin and VDD to keep SRAM power.
VSS	52	I	Digital circuit ground input

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The SPT6601A is equipped with a 16-bit *μ'nSP™*, the newest 16-bit CPU developed by SUNPLUS, pronounced as *micro-n-SP*. Eight registers are involved in *μ'nSP™:* R1 ~ R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP) and, SR (Segment Register). The concatenation of R3 and R4 forms a 32-bit register, MR, which is used as the destination register for multiplication and inner-production. Moreover, Two types of interrupts are FIQ (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software interrupt, BREAK.

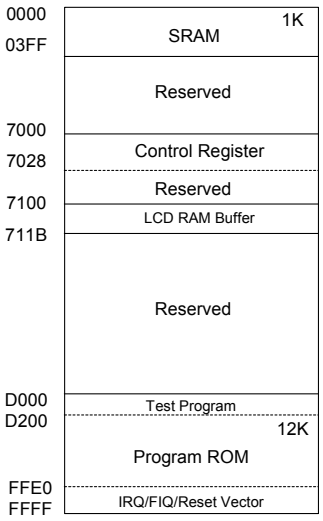
The *μ'nSP™* is a 16-bit microprocessor with 16-bit data and 22-bit address buses. The address bus is capable of addressing 4M bytes of 16-bit data. Not only does the *μ'nSP™* perform general operations such as addition, subtraction and other logical operations, but it also supports multiplication and inner-product operations for digital signal processing. For more information about the *μ'nSP™*, please contact SUNPLUS to obtain the latest documents.

6.2. Memory

ROM: 12K words

RAM: 1K words

6.2.1. Memory Mapping



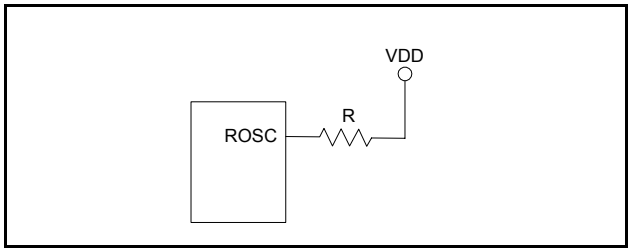
Note: The ROM area of $D000 to $D1FF and $FFE0 to $FFEF is reserved for SUNPLUS internal test program. Available ROM is from $D200 to $FFDF.

6.3. Clock and Operation Mode

6.3.1. Clock

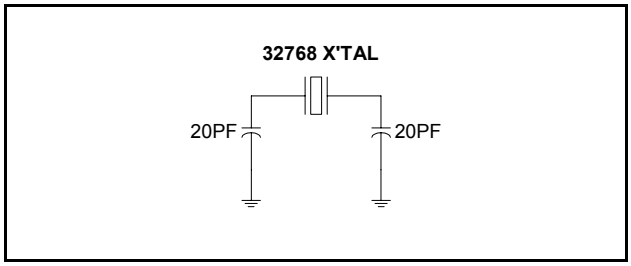
6.3.1.1. System clock

Only one external resistor is required; the unique designed RC-oscillator supports dual operating speed (10MHz / 1MHz) for various applications. For each RC-oscillator, the user can program CPU clock to /1, /2, /4, /8 of oscillator clock output. The default CPU clock is 250KHz (1MHz / 4) after reset or wakeup from sleep mode.



6.3.1.2. 32768 RTC

The 32768Hz X'TAL supplies precise and steady timing for the time-base sources, LCD driver, ADC sampling rate and DTMF generator. The time-base can be utilized for interrupt, wake-up source, timer / counter clock and watchdog timer.



A brief summary of time-base selection is listed in the following tables:

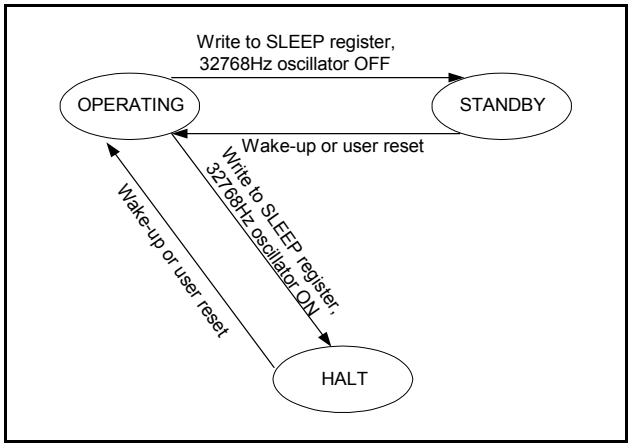
T32kS1	T32kS0	T2kS1	T2kS0
11: T32KHz = 32KHz		11: T2KHZ = 2KHz	
10: T32KHZ = 16KHz		10: T2KHZ = 1KHz	
01: T32KHZ = 8KHz		01: T2KHZ = 512Hz	
00: T32KHZ = 4KHz(Default)		00: T2KHZ = 256Hz(Default)	

T128S1	T128S0	T8S1	T8S0
11: T128HZ = 128Hz		11: T8Hz = 8Hz	
10: T128HZ = 64Hz		10: T8Hz = 4Hz	
01: T128HZ = 32Hz		01: T8HZ = 2Hz	
00: T128HZ = 16Hz(Default)		00: T8HZ = 1Hz(Default)	

6.3.2. Operation Mode

Three Operation modes are available: Operating, Halt and Standby. The following summary depicts the major differences between three modes.

	Operating	Halt	Standby
CPU & ROSC	ON	OFF	OFF
32768Hz OSC.	ON	ON	OFF
LCD Driver	ON	ON	OFF



6.3.2.1. Operating mode

In operating state, functions including CPU, R-oscillator, timer/counter, and LCD controllers are all activated.

6.3.2.2. Halt mode

The user has to enable wakeup sources ($7012) before setting CPU clock control SCK2 - SCK0 (in Register $7015) to "111" to enter halt mode. In halt mode, the 32768Hz oscillator must be enabled if the time-base wakeup is selected.

6.3.2.3. Standby mode

To enter standby mode, set CKS2 - CKS0 = "111" and disable 32768Hz crystal oscillator. In standby mode, all functions are shut down, but RAM and I/O continue to remain in the previous states. The power consumption is minimized in standby mode. For any wakeup event occurs during the halt or standby mode, the device will execute instruction from the beginning of the program (warm start).

6.4. Interrupt

Setting or clearing the Interrupt Control Register ($7010) can enable or disable the service of the corresponding interrupt function. Once an interrupt event occurs, the CPU will enter its interrupt service sub-routine if related interrupt flag is enabled. Be sure that all interrupts must be disabled before entering sleep mode. Interrupt vectors in SPT6601A are summarized in the following table:

Vector	Address	Interrupt Source	Priority
FIQ	FFF6	IOC1INT	Higher
IRQ0	FFF8	IOCOINT / RINGDET	
IRQ1	FFF9	IOAKEY	
IRQ2	FFFA	TMAOC	
IRQ3	FFFB	TMBOC	
IRQ4	FFFC	T32Khz	
IRQ5	FFFD	T2kHz	
IRQ6	FFFE	T128Hz	
IRQ7	FFFF	T8Hz	Lower

Note: If more than one IRQ occurs simultaneously, the first priority is IRQ0; the 2nd priority is IOR1 and…etc. The IRQ7 holds the lowest priority. However, a higher priority IRQ cannot take over a lower priority IRQ if the lower one occurs before the higher IRQ. The priority applies only when two IRQs occur concurrently.

6.5. Wakeup

Similar to interrupt function, three are five wake-up sources: IOA[7:0] key change wake-up, IOC[1:0] input change wake-up, Ringer Detect, TimerA/B overflow wake-up and T32kHz/T2kHz/T128Hz/T8Hz. For instance, suppose TimerA control registers are enabled and 32768Hz is selected as the clock source, the Timer/Counter can work individually without extra attention. The CPU can awake only when an overflow signal occurs. After the device awakes from halt or standby state, it will execute instruction from the beginning of the program. Memory, control registers and I/O status will all remain in previous states.

6.6. RESET

6.6.1. RESET pin

The control registers and CPU are initialized when reset pin receives a low signal, but the data in SRAM will not be changed. A 0.1μF capacitor is required crossing on RESET pin and GND.

6.6.2. PORN and LVR

A Power-On-Reset (POR) and a Low Voltage Reset (LVR) are available in the SPT6601A. Once POR or LVR activates, the SPT6601A will be reset and the CPU will start executing from the beginning of the program (cold start).

6.6.3. Watchdog timer (WDT)

The external Watchdog Timer (WDT) is designed for recovering system from abnormal operation. If the system is halted for more than one second, WDT generates a system reset to restart system. If WDT is enabled, the WDT must be cleared within every 2 seconds to avoid accidental reset. Note that the WDT only works when 32768Hz clock is activated.

6.7. I/O

There is a total of 26-bit programmable bi-directional I/O ports (IOA [7:0], IOB[7:0], IOC[7:0] and IOD[1:0]) in SPT6601A. Each pin can be programmed individually to pure output buffer, ODP (open drain PMOS), ODN (open drain NMOS), pure input buffer, input with pull-low or input with pull-high. The IOs also have alternative functions. The IOA and IOC[1:0] can be used as wakeup / interrupt sources. Furthermore, IOD1 can be programmed as tone output.

Please refer to the *SPT6601A programming guide -- I/O Configuration* for more information.
Finally, make sure that all I/Os are set as input mode without pull high / pull low after RESET.

6.8. LCD Driver

SPT6601A offers a LCD controller and driver for a maximum of 224 dots LCD display (1/4 bias, 1/8 duty). In power-on state, LCD display is off in default mode. The user can activate LCD display and define the LCD configuration (bias, duty, display mode) through software programming. Once the LCD configuration is initialized, the desired pattern can be displayed by filling the LCD RAM buffer with appropriated data. The LCD driver can operate automatically even the system is in halt mode (if 32768Hz oscillator keep running).

Furthermore, the built-in LCD voltage regulator can optimize the LCD contrast control. Also, the programmer can turn off the LCD display through LCD Control Register to save power.

6.9. AGC and ADC

6.9.1. AGC

The Register, $7026, controls the digital gain of the built-in OP AMP. The available gains are x1/3, x2, x8 and x32 and the AGC output is sent into an 8-bit ADC.

6.9.2. ADC

The external 8-bit Analog-to-Digit Converter (ADC) is software controllable. Plus, the ADC sampling rate can be determined by the overflow signal of Timer A. The default of ADC sampling rate is 8192Hz.

Note: In any mode, the sampling rate must be equal or less than 8192Hz.

6.10. DTMF GENERATOR

The SPT6601A provides two current DACs that serve as the Dual-Tone-Multi-Frequency (DTMF) generators, and speech or melody generators. The generator is capable of producing the following DTMF signals by software programming.

	C0	C1	C2	C3	
R0	1	2	3	A	---- 697Hz
R1	4	5	6	B	---- 770Hz
R2	7	8	9	C	---- 852Hz
R3	*	0	#	D	---- 941Hz
	1209	1336	1477	1633 Hz	

Note: Be sure to disable DACs to save power when the DTMF generator is not needed.

6.11. Ring Detector

A Ring / Line-Reversal Detector, controlled by Register $7028, is built-in the SPT6601A. If the detector is required, the application circuit related to pin RDRC and RDIN must be added. The detector dissipates only transition current and can be always turned on. To satisfy various applications, both rising and falling transitions on pin RDRC can be programmed as interrupt or wake-up source.

6.12. Timer A / B and Tone Output

6.12.1. Timer A / B

The SPT6601A provides a 16-bit TimerA and an 8-bit Timer B. The overflow signal of TimerA or TimerB can be used as interrupt / wakeup sources, and be used to determine ADC sampling rate (only timer A) and the tone output frequency. A variety of signals can be chosen for clock sources of Timer A and TimerB. Please refer to *SPT6601A Programming Guide* for more information.

6.12.2. Tone Output

Normally, the pin IOD1 behaves as a normal I/O. While $700E bit 5 is set to “1”, IOD1 behaves as a tone output pin, in which frequency is determined by Timer A or TimerB overflow signal.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 3.6V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

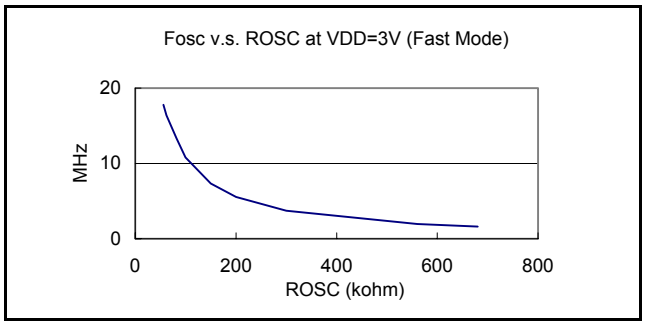
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 3.0V, T_A = 25℃)

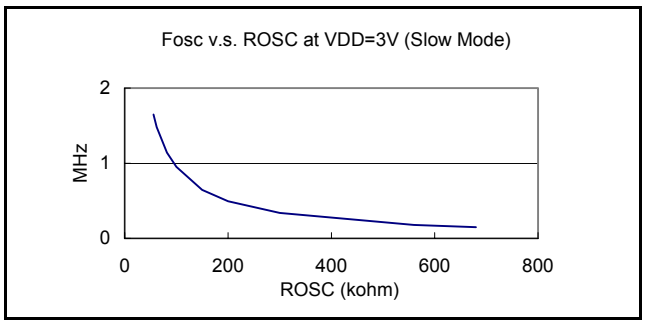
Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage 1	VDD	2.0	-	3.6	V	For Pulse/Tone dialer operation
Operating Voltage 2	VDD	2.2	-	3.6	V	For CID signal receiving
Operating Current 1	I_{OP1}	-	200	-	μA	F_{CPU} = 250KHz @ 3.0V, no load For Pulse dial
Operating Current 2	I_{OP2}	-	400	-	μA	F_{CPU} = 250KHz @ 3.0V, no load For Tone dial
Operating Current 3	I_{OP3}	-	2250	-	μA	F_{CPU} = 10MHz @ 3.0V, no load For CID signal receiving
Halt Mode Current	I_{HALT}	-	20	-	μA	Active 32768Hz OSC, LCD display on without panel loading, ROSC off
Standby Current	I_{STBY}	-	-	1.0	μA	ROSC off, 32768Hz off
Output High Current (IOC[5:0], IOD1)	I_{OH}	-5.0	-	-	mA	VDD = 3.0V V_{OH} = 2.4V
Output Sink Current (IOB[7:6], IOC[7:0], IOD1)	I_{OL}	5.0	-	-	mA	VDD = 3.0V V_{OL} = 0.4V
Output High Current (IOA[7:0], IOB[5:0], IOD0)	I_{OH}	-1.0	-	-	mA	VDD = 3.0V V_{OH} = 2.4V
Output Sink Current (IOA[7:0], IOB[5:0], IOD0)	I_{OL}	2.0	-	-	mA	VDD = 3.0V V_{OL} = 0.4V
Pull High Resistor (IOA[7:0])	R_{HIGH}	-	200	-	KΩ	VDD = 3.0V
Pull Low Resistor (IOA[7:6])	R_{LOW}	-	200	-	KΩ	VDD = 3.0V
ROSC Frequency (Fast)	F_{OSCH}	-	10	-	MHz	VDD = 3.0V, R_{OSC} = 100KΩ
ROSC Frequency (Slow)	F_{OSCL}	-	1.0	-	MHz	VDD = 3.0V, R_{OSC} = 100KΩ

7.3. The Relationships Between the R_{OSC} and the F_{OSC}

7.3.1. Fast mode, VDD = 3.0V, T_A = 25℃

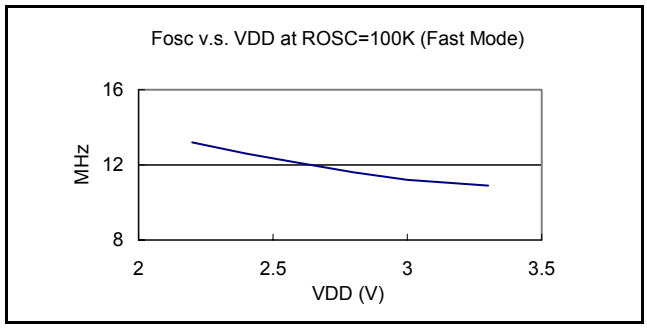


7.3.2. Slow mode, VDD = 3.0V, T_A = 25℃

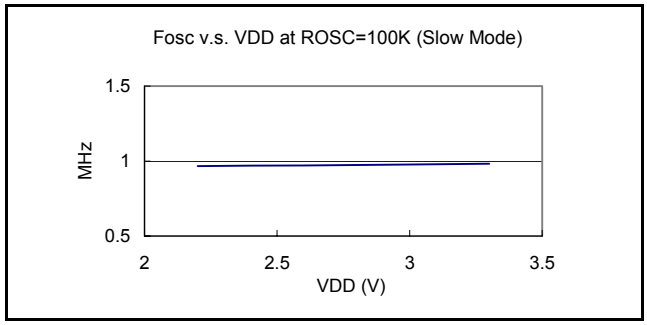


7.4. The Relationships Between the F_{OSC} and VDD

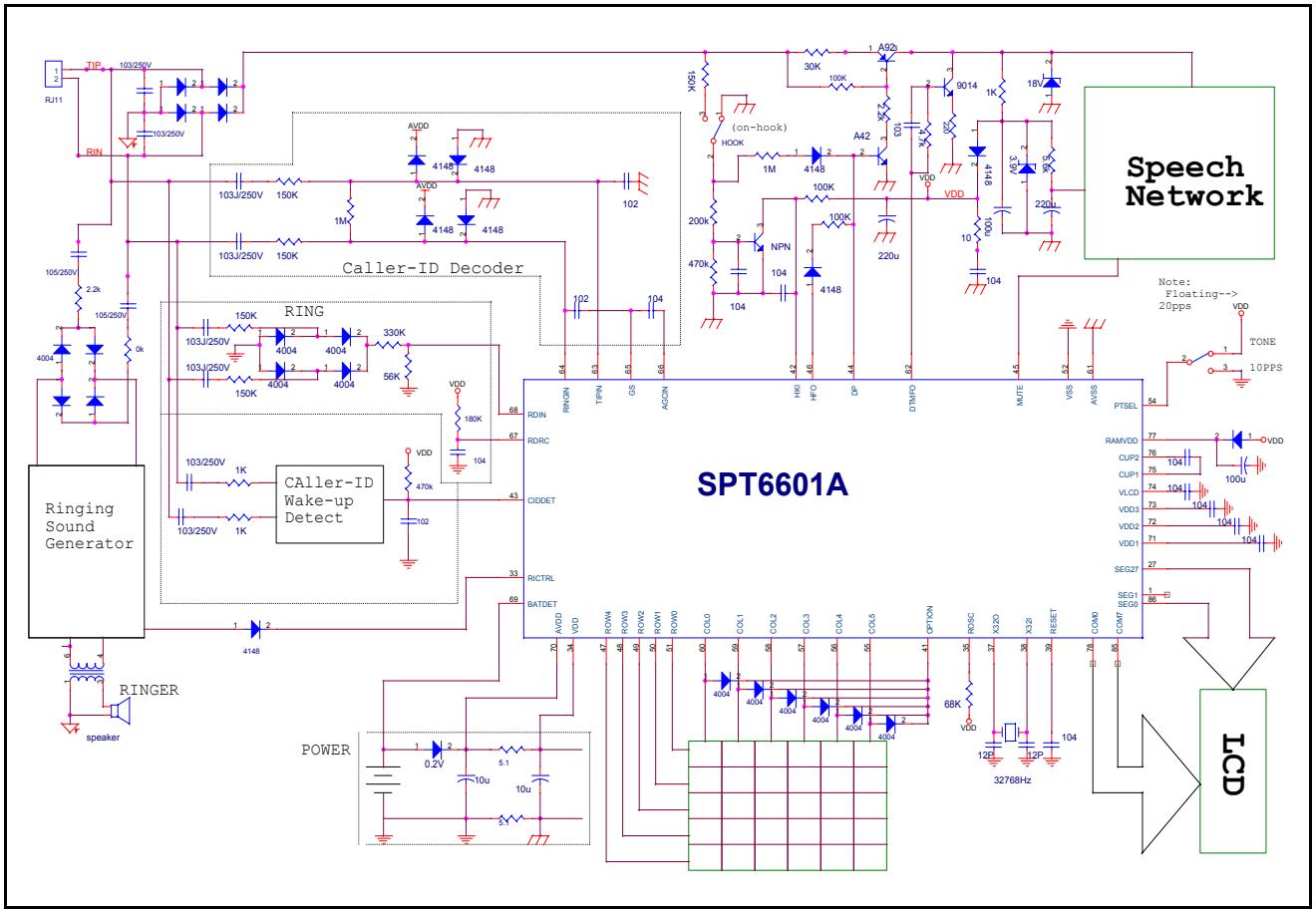
7.4.1. Fast mode, R_{OSC} = 100KΩ, T_A = 25℃



7.4.2. Slow Mode, ROSC = 100KΩ, TA = 25℃

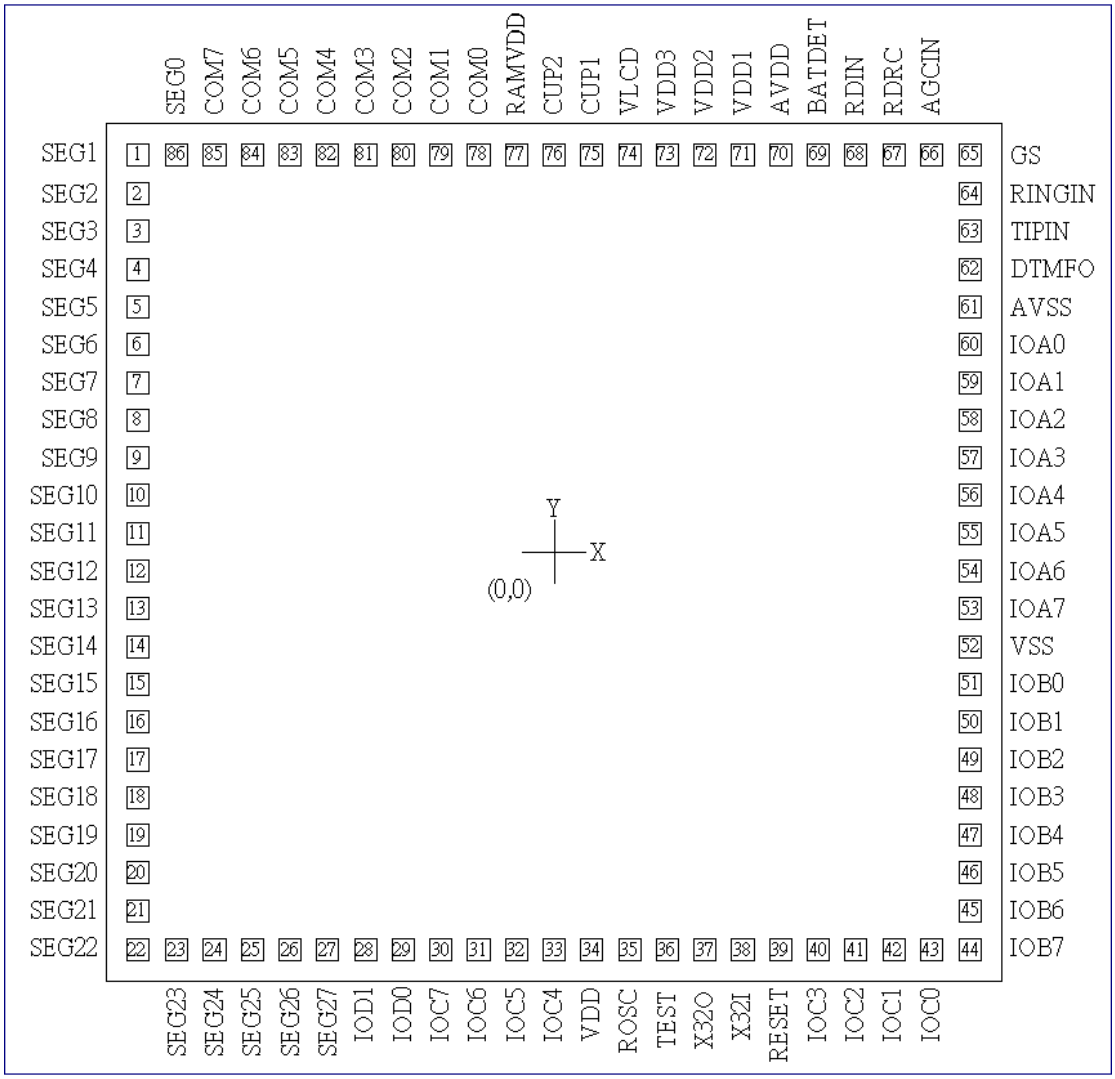


8. APPLICATION CIRCUITS



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 2950μm x 2880μm

This IC substrate must be connected to VSS

Note1: Chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPT6601A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	SEG1	-1325	1265	41	IOC2	960	-1265
2	SEG2	-1325	1140	42	IOC1	1080	-1265
3	SEG3	-1325	1020	43	IOC0	1200	-1265
4	SEG4	-1325	900	44	IOB7	1325	-1265
5	SEG5	-1325	780	45	IOB6	1325	-1140
6	SEG6	-1325	660	46	IOB5	1325	-1020
7	SEG7	-1325	540	47	IOB4	1325	-900
8	SEG8	-1325	420	48	IOB3	1325	-780
9	SEG9	-1325	300	49	IOB2	1325	-660
10	SEG10	-1325	180	50	IOB1	1325	-540
11	SEG11	-1325	60	51	IOB0	1325	-420
12	SEG12	-1325	-60	52	VSS	1325	-300
13	SEG13	-1325	-180	53	IOA7	1325	-180
14	SEG14	-1325	-300	54	IOA6	1325	-60
15	SEG15	-1325	-420	55	IOA5	1325	60
16	SEG16	-1325	-540	56	IOA4	1325	180
17	SEG17	-1325	-660	57	IOA3	1325	300
18	SEG18	-1325	-780	58	IOA2	1325	420
19	SEG19	-1325	-900	59	IOA1	1325	540
20	SEG20	-1325	-1020	60	IOA0	1325	660
21	SEG21	-1325	-1140	61	AVSS	1325	780
22	SEG22	-1325	-1265	62	DTMFO	1325	900
23	SEG23	-1200	-1265	63	TIPIN	1325	1020
24	SEG24	-1080	-1265	64	RINGIN	1325	1140
25	SEG25	-960	-1265	65	GS	1325	1265
26	SEG26	-840	-1265	66	AGCIN	1200	1265
27	SEG27	-720	-1265	67	RDRC	1080	1265
28	IOD1	-600	-1265	68	RDIN	960	1265
29	IOD0	-480	-1265	69	BATDET	840	1265
30	IOC7	-360	-1265	70	AVDD	720	1265
31	IOC6	-240	-1265	71	VDD1	600	1265
32	IOC5	-120	-1265	72	VDD2	480	1265
33	IOC4	0	-1265	73	VDD3	360	1265
34	VDD	120	-1265	74	VLCD	240	1265
35	ROSC	240	-1265	75	CUP1	120	1265
36	TEST	360	-1265	76	CUP2	0	1265
37	X32O	480	-1265	77	RAMVDD	-120	1265
38	X32I	600	-1265	78	COM0	-240	1265
39	RESET	720	-1265	79	COM1	-360	1265
40	IOC3	840	-1265	80	COM2	-480	1265
81	COM3	-600	1265	84	COM6	-960	1265
82	COM4	-720	1265	85	COM7	-1080	1265
83	COM5	-840	1265	86	SEG0	-1200	1265

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
APR. 30, 2001	0.1	Original	15